CN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,343	01/30/2002	Toshitake Yaegashi	219030US2S	5195

22850 7590 09/10/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/058,343	Applicant(s) YAEGASHI, TOSHITAKE	
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-17,20,21,24,26-32 and 35-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,22,25,33 and 34* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☒ Claim(s) *1-37* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 219030US2S

Filing Date: 1/30/2002

Claimed Foreign Priority Dates: 3/23/2001 (JP 2001-85821)
1/31/2001 (JP 2001-23973)

Applicant(s): Yaegashi

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the election in paper no. 9 filed on 7/21/2003.

Election

1. Applicant's election without traverse of species #2, as it was indicated in paper no. 7, mailed on 5/23/2003, is acknowledged. The applicant indicates that claims 1, 3, 4, 6, 7, 11, 12, 18, 19, 22, 23, 25-27, 31, 33, and 34 read on species #2.

2. Claim 1, however, recites that the source region of the selection transistor is asymmetrical with respect to the shape of the drain region below the selection transistor. This limitation does not read on species #2 but on species #1, as it was indicated in paper no. 7. Accordingly, claims 1, 3, 4, 6, and 7 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

3. Claim 8 recites that the channel regions of the selection transistors have different impurity concentrations at positions having the same depth from the boundary between the semiconductor substrate and a gate insulation film. This limitation reads on species #1 instead of species #2. Accordingly, claims 11 and 12 are withdrawn from further

consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

4. Claim 26 recites that each of the selection transistors has a portion in which the impurity concentration of the channel region is different in a gate length direction at equal depths from the boundary between the substrate and the gate insulation film. This limitation reads on species #1 rather than on species #2. Accordingly, claim 26 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

5. Claim 27 recites that the source region of each of the selection transistors is different from that of the drain region at equal depths from the boundary between the substrate and the gate insulation film, and that the source/drain diffusion region connected to the bit line has a lower effective impurity concentration that that of the source/drain diffusion region of the memory cell. This limitation reads on species #1 rather than on species #2. Accordingly, claims 27 and 31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters **14** (pp.71/ll.15) and **54** (pp.71/ll.22) have both been used

to designate the channel region of a selection gate transistor. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 18, 19, 22, 25, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi (US 4939690) in view of Tobita (US 5646516).

11. Regarding claim 18, Momodomi shows (see, *e.g.*, figs. 1 and 4) most aspects of the instant invention including a non-volatile semiconductor memory device comprising:

- a plurality of memory cell units $\mathbf{B_{ij}}$ comprising at least one memory cell $\mathbf{M_{11}}$ having a laminated gate structure of a charge accumulation layer **28** and a control gate layer **32** formed on a semiconductor substrate **10** through a gate insulation layer
- a plurality of selection gate transistors $\mathbf{Qs_{ij}}$, each of which having a gate electrode **36** formed through the gate insulation film and two source/drain

diffusion layers, one **16** of which is connected to one of the memory cell units B_{ij} and the other **14** of which is electrically connected to a bit line BL_1**(42)** or a source line

wherein the plurality of selection transistors Qs_{ij} include a pair of first selection transistors disposed in confrontation with each other across a contact portion connected to the bit line BL_1 of the source line and having substantially the same structure.

Momodomi, however, fails to specify that the channel regions of the pair of selection transistors have the same impurity concentration in a gate length direction at equal depths from the boundary between the semiconductor substrate and the gate insulation film, and that the concentration distribution of impurity in the channel regions of the pair of selection gate transistors is different from that of the channel region of the memory cell.

Tobita (see, *e.g.*, col.33/ll.65-col.34/ll.23), on the other hand, teaches that typically the selection transistors will have the same impurity concentrations and that the concentration distribution of impurity of the selection transistors will conventionally be different than that of the memory cells.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have the channel regions of the pair of selection transistor of Momodomi having the same impurity concentrations in a gate length direction at equal depths from the boundary between the semiconductor substrate and the gate insulation film, since, as taught by Tobita, these characteristics are typical of semiconductor memory devices.

12. Regarding claim 22, Tobita shows (see, *e.g.*, col.3/ll.65-col.34/ll.23) that the impurity concentration of the channel region of each of the selection transistors is made higher than that of the channel region of the memory cell.

13. Regarding claim 25, Momodomi shows (see, *e.g.*, fig. 4) that the junction depth of the source/drain diffusion layer **14** of each of the first selection transistors is smaller than the junction depth of the source/drain diffusion layer **16** of the memory cell $\mathbf{M_{11}}$.

14. Regarding claim 34, Momodomi shows (see, *e.g.*, fig. 4) that a part of the source/drain diffusion layer of each selection transistor and a part of the source/drain diffusion layer have such a structure that they are connected to each other through a continuous activation region without being isolated from each other by an element isolation region.

15. Regarding claim 19, Momodomi shows (see, *e.g.*, figs. 1 and 4) most aspects of the instant invention including a non-volatile semiconductor memory device comprising:

- a plurality of memory cell units $\mathbf{B_{ij}}$ comprising at least one memory cell $\mathbf{M_{ij}}$ having a laminated gate structure of a charge accumulation layer **28** and a control gate layer **32** formed on a semiconductor substrate **10** through a gate insulation film
- a plurality of selection gate transistors $\mathbf{Qs_{ij}}$ each having a gate electrode **36** formed through a gate insulation film and two source/drain diffusion layers, one **16** of which is connected to a memory cell unit $\mathbf{M_{11}}$ and the other **14** of which is electrically connected to a bit line $\mathbf{BL_1(42)}$ of a source line

wherein the plurality of selection transistors $\mathbf{Qs_{ij}}$ have a pair of first selection transistors disposed in confrontation with each other across a contact portion connected to the bit line $\mathbf{BL_1}$ or the source line and having substantially the same structure

16. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi in view of Tobita and Momotomi (JP 2000-68487).

17. Regarding claim 33, Momodomi/Tobita shows most aspects of the instant invention (see paragraphs 11-15 above), except for the distance between the gate electrode of each of the selection transistors and the gate electrode of the memory cell being larger than the distance between the gate electrodes of the memory cells. Momotomi (see, *e.g.*, fig. 8 and abstract), however, teaches that doing so will eliminate the influence on the neutral threshold voltage by the substrate bias effect during reading.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have a larger distance between the gate electrode of each of the selection transistors and the gate electrode of the memory cell than the distance between the gate electrodes of the memory cells of Momodomi/Tobita, as suggested by Momotomi, to eliminate the influence on the neutral threshold voltage by the substrate bias effect during reading of the memory device.

Allowable Subject Matter

18. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

19. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

21. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

22. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314-326,390-393,401; 438/258,266	9/4/2003
Other Documentation: PLUS Analysis	9/4/2003
Electronic Database(s): EAST (USPAT, EPO, JPO, PGPub)	9/4/2003

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

MDP/mdp
September 4, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800